Microstructures

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Supplementary Material

Microstructural origin of dual band emission and thermal dynamics in suspended silicon-on-insulator infrared sources

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MATERIALS AND METHODS

Numerical Simulation

Electrothermal and thermomechanical simulations were conducted in Simulation platform using coupled Thermal-Electric and Static Structural modules, with thermal results mapped as mechanical boundary conditions. The main heat transfer Equations are given by the following equations:

$$\rho C_p \frac{\partial T}{\partial t} + \nabla(-k\nabla T) = Q \tag{S1}$$

$$Q = \sigma|\nabla V|^2 = \frac{\sigma_0}{1+\beta(T-T_R)}|\nabla V|^2 \tag{S2}$$

$$\varepsilon = \varepsilon_0 + \varepsilon_{th} = \varepsilon_0 + \alpha(T-T_R) \tag{S3}$$

In **Equation (S1)**, ρ is the material density [kg/m³], C_p is the specific heat capacity [kg/m^3], T is the temperature [K], k is the thermal conductivity [W/(m·K)], and Q is the volumetric heat generation rate [W/m³]. Equation (1) can be alternatively expressed as **Equation (S2)**, where the electrical conductivity σ is a function of temperature T, σ_0 is the conductivity at the reference temperature T_R, β is the temperature coefficient of resistance (TCR), and ∇V is the electric potential gradient. When a temperature field is applied to a mechanical structure, it induces a thermal deformation. The total deformation is expressed by **Equation (S3)**. Where ε is the total deformation of the infrared light source, ε_0 is the initial deformation in the absence of applied voltage, ε_{th} is the thermal expansion deformation induced by the temperature difference, and α is the coefficient of thermal expansion (CTE) of the material [1/K].

The 3D structural model was imported into the simulation platform for subsequent analysis. The relevant geometric parameters of the model are listed in **Supplementary Table 1**. Furthermore, the material properties must be incorporated to solve the mathematical equations embedded within the respective modules, as shown in **Supplementary Table 2**. To facilitate the simulation, suspended, semi-closed, and closed membrane structures were simplified. Specifically, the boron-diffused single-crystal silicon layer and oxide layer above the polysilicon were excluded from the model. Thermal convection and radiation are considered to occur at the outer surface of the infrared light source. The ambient temperature was set to 27.8 °C, the surface emissivity of the polysilicon thin film was set to 0.8, and the convection was set to 10 W/(m^2·K). The aluminum electrodes were biased at 12 V, and the bottom surface of the Si substrate was assigned a fixed constraint. The simulations can be calculated under Dirichlet, Neumann, and mixed boundary conditions numerically in the 3D-finite element method (FEM) model with a tetrahedral mesh.

Materials and fabrication

(a) Using nitrogen N2 as the protective gas, the SOI substrate was placed in a tube furnace at 1050 °C for 5.5 h of B ion pre-deposition, followed by the removal of the resulting borosilicate glass (B_2O_3) using a buffered oxide etchant (BOE) solution under dark conditions. The substrate was then heated to 1150 °C for boron redistribution for 7 h. The heavy boron diffusion concentration was approximately 7×10^{19} cm^{-3}, and the sheet resistance measured by a four-point probe resistance tester (D41-11A/ZM, China) was 1.3003 Ω/□. (b) A thermal oxide layer was grown on the SOI substrate by wet oxidation at 1050 °C for 50 min. The thickness of the SiO_2 thermal oxide layer was measured to be 500 ± 50 nm with a film thickness measuring instrument(BRUKER Dektak XTL, USA). (c) A polycrystalline silicon (poly-Si) thin film was deposited by

low-pressure chemical vapor deposition (LPCVD) at 600 °C in a furnace tube with 100 sccm of SiH_4 gas for 1 h, with a measured thickness of 500 ± 30 nm. Subsequently, a 100 ± 5 nm SiO_2 thermal oxide layer was grown on the poly-Si layer by dry oxidation at 1050 °C for 30 min. (d) Boron ions were implanted into the polycrystalline silicon at 110 keV with a 7° tilt angle and a dose of 5×10^{15} cm^{-2}, followed by annealing at 950 °C for 45 s in a rapid thermal processing (RTP) furnace. (e) A5214 positive photoresist was spin-coated (2500 r/min, 30 s) and prebaked (95 °C, 2 min), then exposed for 15 s (MA8 photolithography system, SUSS, Germany) and developed for 50 s to form rectangular poly-Si patterns. The SiO_2 and poly-Si layers were etched by plasma etching (40 s) and deep silicon etching (12 s), respectively, yielding the poly-Si radiation layer boss structures. (f) Using the same photolithography process as aforementioned, the Al electrode window patterns were defined, and the SiO_2 layer within the electrode windows was etched by plasma etching for 40 s. Titanium with a thickness of 50 nm was deposited by electron beam evaporation as an adhesion layer, followed by the deposition of aluminum with a thickness of 1500 ± 50 nm. The aluminum electrodes were then formed by ultrasonic lift-off in an acetone bath for 15 min. The electrodes were finally annealed at 400 °C for 3 min in a RTP furnace. (g) A6130 positive photoresist was spin-coated (1500 r/min, 30 s) and prebaked (95 °C, 2 min), then exposed for 30 s (MA8 photolithography system, SUSS, Germany) and developed for 70 s to pattern isolation trenches on both sides of the poly-Si radiation layer. Plasma etching (230 s) was applied to the SiO_2 electrothermal isolation layer, deep silicon etching (450 s) to the top heavily boron-doped Si layer, and plasma etching (280 s) to the buried SiO_2 layer of the SOI substrate. (h) Using the same photolithography process as aforementioned, rectangular cavity structures were defined on the backside of the SOI substrate. Deep Reactive Ion Etching (DRIE) was performed for 30 min to fabricate semi-closed membrane infrared light source chips, and 60 min of DRIE yielded suspended membrane infrared light source chips. Furthermore, the wafers were subjected to standard RCA cleaning prior to each fabrication process.

RESULTS AND DISCUSSION

Electrical-to-Optical Conversion Efficiency

The electrical-to-optical conversion efficiency is a critical metric for evaluating the radiative efficiency of an infrared light source. **Supplementary Table 3** presents the electro-optical conversion efficiency of the suspended membrane infrared source. The measurement of the electro-optical conversion efficiency η_{eo} for the MEMS infrared source involves the driving power P_d, continuous-band spectral irradiance $M_{\lambda_1 \sim \lambda_2}(T)$ and radiating area S. The product of the continuous-band spectral radiant exitance and radiating area yields the infrared radiative power P_{IR}. This relationship is given by **Equation (S4)**:

$$\eta_{eo} = \frac{P_{IR}}{P_d} \times 100\% = \frac{M_{\lambda_1 \sim \lambda_2}(T)S}{V_D I_D} \times 100\% \quad \text{(S4)}$$

where V_D and I_D are the driving voltage and current of the infrared light source, respectively. As shown in **Supplementary Table 3**, with an increase in V_D, both the radiative and driving powers increase simultaneously, but the growth rate of the radiative power is higher than that of the driving power, leading to an improvement in the electro-optical conversion efficiency. When the driving voltage was 7 V, the electro-optical conversion efficiency reached 12.33%.

Thermal Stability

Thermal stability tests were performed on both suspended and semi-closed membrane infrared source chips using a microscope coupled with an in-situ probe station. The chip was heated in a N_2 atmosphere using an in-situ heating stage. The temperature was increased at a rate of 25 °C/min. Upon reaching 300 °C, 450 °C, and 600 °C, the temperature was held isothermally for 1 min at each plateau. Finally, the sample was allowed to cool naturally to room temperature. The polysilicon emission layer of the semi-closed membrane infrared source chip exhibited robust thermal stability at 300 °C, 450 °C, and 600 °C, with no significant film deformation observed under the microscope. During the heating process, thermal expansion deformation of the silicon substrate in the semi-closed membrane infrared light source chip was observed under the microscope, accompanied by the displacement of the chip on the probe station. However, the polysilicon light-emitting layer of the suspended membrane infrared source chip was observed to deform downward, assuming a pronounced V-shaped configuration. Nevertheless, the film did not reach its bending limit and demonstrated good thermal stability at its operating temperature of 450 °C. The isolation trenches on both sides of the polysilicon radiation layer and the back cavity structures confine heat inside the film, leading to thermal deformation occurring on the film instead of the substrate. However, when the temperature was elevated to 600 °C, cracks formed at the junction between the film and the silicon substrate in the suspended region due to excessive deformation, which would compromise the film's service life. The thermal stability test procedure is provided in the **Supplementary Video**.

Supplementary Table 1. Simulation parameter for the coupling model

Parameters	Length (μm)	Width (μm)	Thickness (μm)
Si substrate	3700	3700	400
Poly-Si thin film	3200	1900	0.5
Aluminum electrode	1900	250	1.5
Cavity (suspended membrane)	2800	2800	400
Cavity (Semi-closed membrane)	2800	2800	200

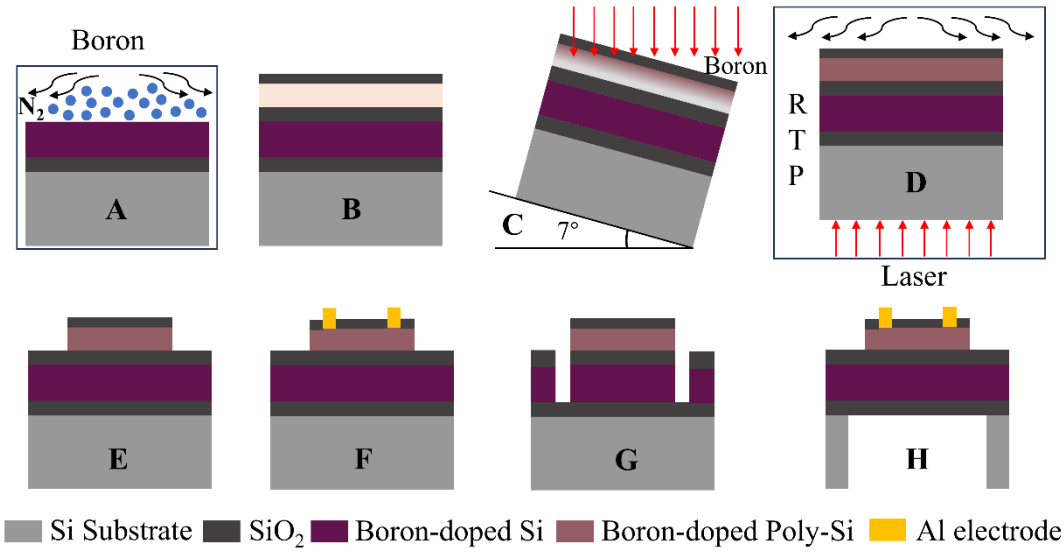
Supplementary Table 2. Material properties used for the simulation

Parameters	Single Crystal Silicon	Polycrystalline Silicon	Aluminum
Density	2329 kg/m3	2320 kg/m3	2700 kg/m3
Young's modulus	170×10^9 Pa	160×10^9 Pa	7×10^{10} Pa
Poission's ratio	0.27	0.23	0.35
Thermal expansion coefficient	$2.6 \times 10^{-6}\,K^{-1}$	$2.6 \times 10^{-6}\,K^{-1}$	$2.31 \times 10^{-5}\,K^{-1}$
Heat capacity	700 J/(kg·K)	678 J/(kg·K)	904 J/(kg·K)
Thermal conductivity	131 W/(m·K)	34 W/(m·K)	237 W/(m·K)
Resistivity	1×10^4 (Ω·m)	2.07×10^{-5}(Ω·m)	2.82×10^{-8} (Ω·m)

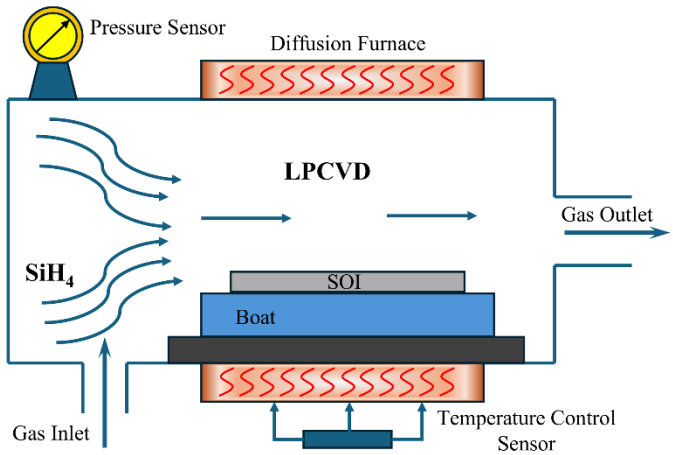
Supplementary Table 3. Electro-optical conversion efficiency

V_D (V)	P_d (mW)	P_{IR} (mW)	η_{eo} (%)
5	533.8	22.47	4.21
5.5	589.4	37.90	6.43
6	715.9	74.38	10.39
6.5	784.3	92.23	11.76
7	885.7	109.21	12.33

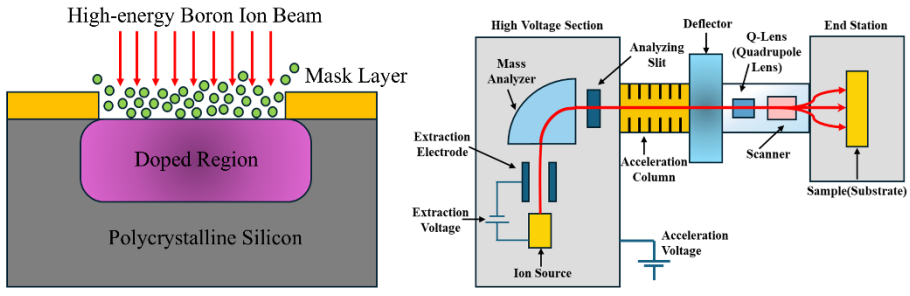
V_D : driving voltage; P_d : driving power;: P_{IR} infrared radiative power; η_{eo} : electro-optical conversion efficiency.



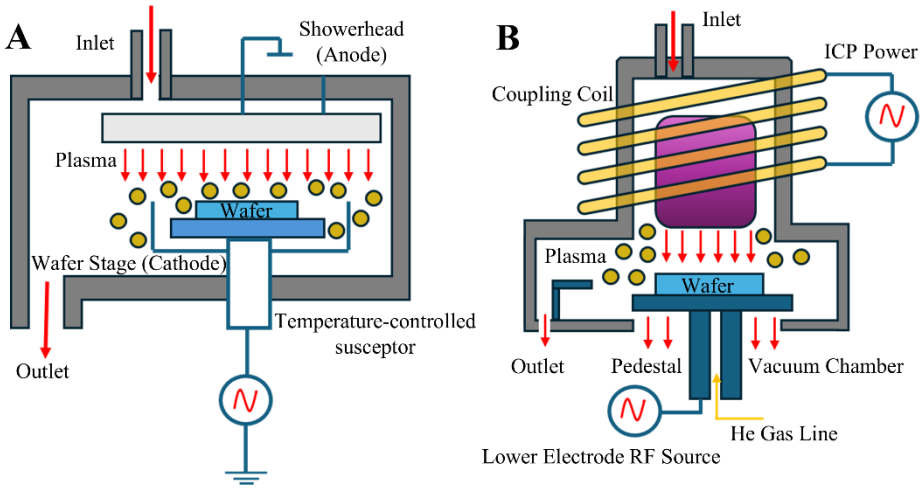
Supplementary Figure 1. Fabrication process of MEMS infrared light source chip. (A) Heavy boron diffusion on single crystalline Si; (B) Deposited SiO_2, Poly-Si and SiO_2 in sequence; (C) Boron ion implantation into Poly-Si; (D) Ion implantation annealing; (E) Etching SiO_2 and Poly-Si; (F) Evaporating Al electrodes; (G) Etching Poly-Si side windows; (H) Etching the backside cavity.



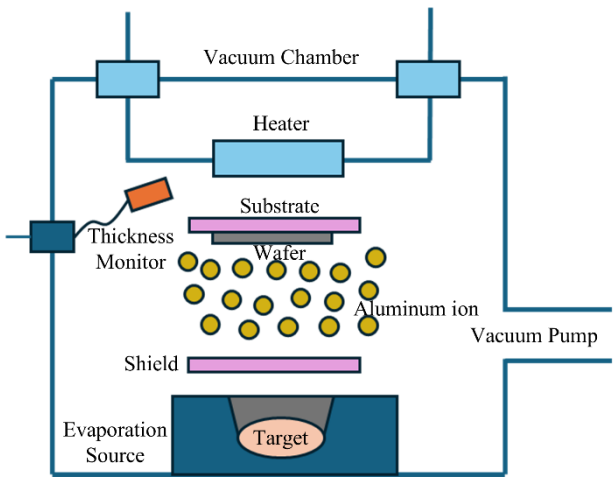
Supplementary Figure 2. Schematic illustration of polycrystalline silicon growth by LPCVD.



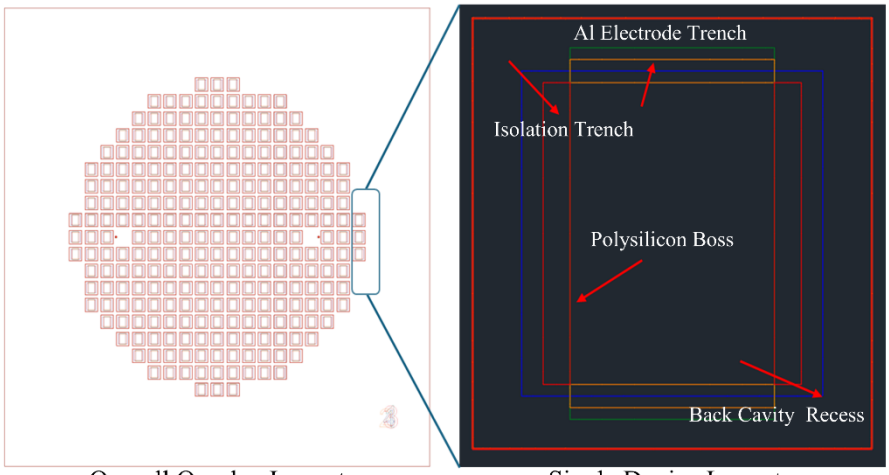
Supplementary Figure 3. Schematic of boron ion implantation into polycrystalline silicon.



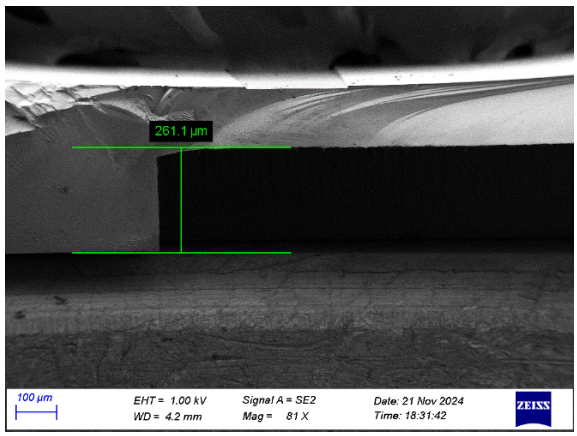
Supplementary Figure 4. Schematic illustration of the dry etching mechanism. (A) ICP etching of silicon dioxide; (B) DRIE deep silicon etching.



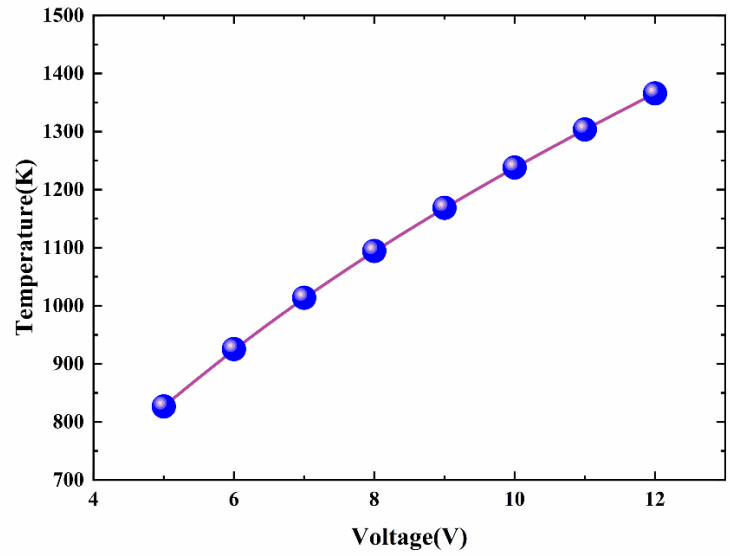
Supplementary Figure 5. Aluminum electrode fabrication via ion beam evaporation.



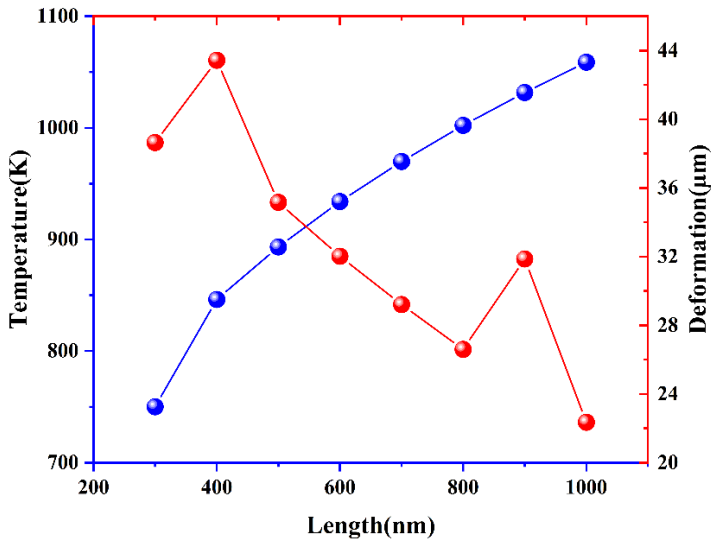
Supplementary Figure 6. Photomask patterns for the MEMS infrared light source.



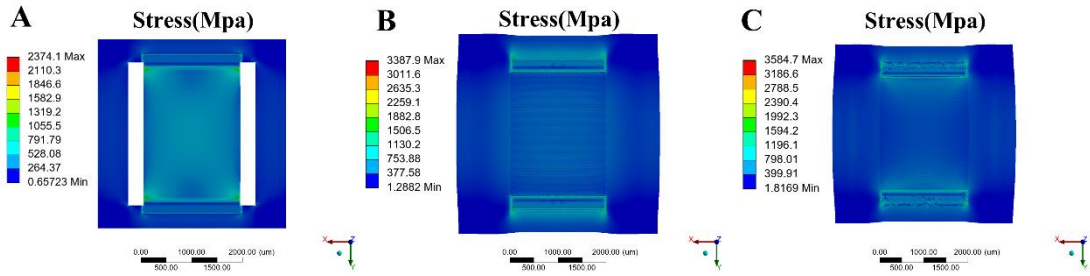
Supplementary Figure 7. Back-side dry-etched structure of the semi-closed membrane infrared light source chip.



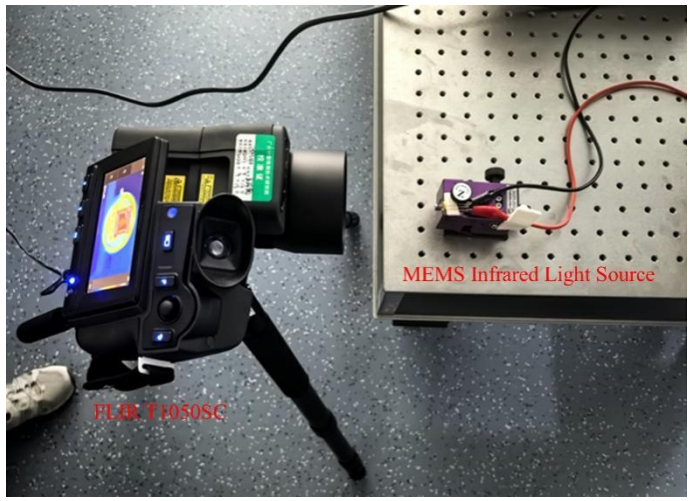
Supplementary Figure 8. Curves of radiative temperature versus driving voltage for the suspended membrane infrared source chip.



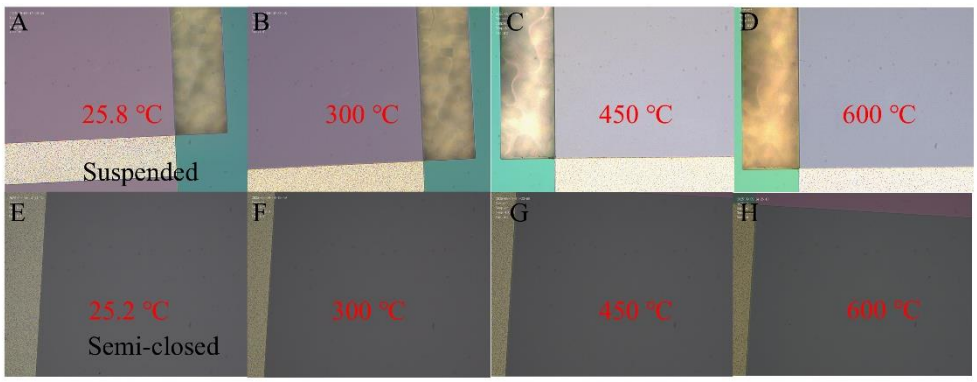
Supplementary Figure 9. Radiative temperature and thermal deformation of the suspended infrared source as a function of polysilicon layer thickness.



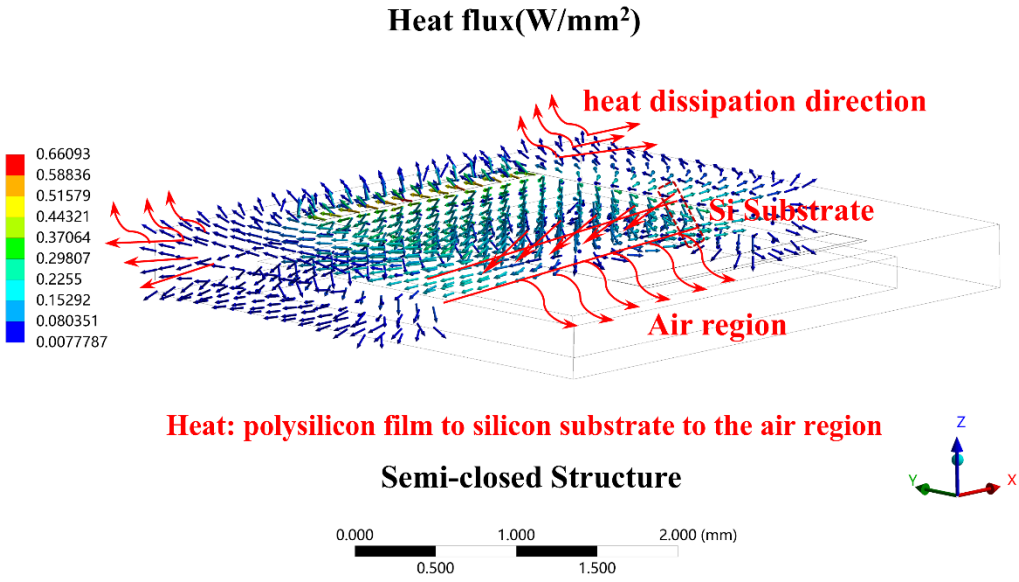
Supplementary Figure 10. (A-C) Stress distribution and deflection for suspended membrane, semi-closed membrane and closed membrane.



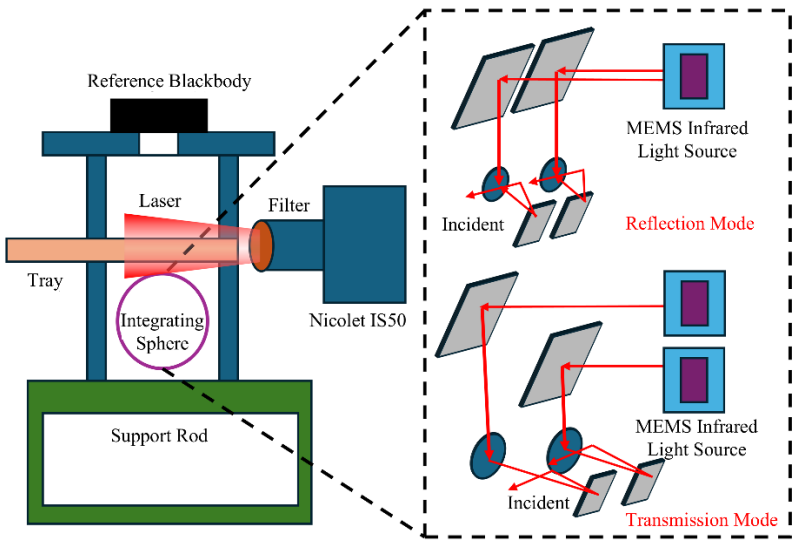
Supplementary Figure 11. Experimental platform for electrothermal characterization of the infrared light source. This figure was taken by the authors.



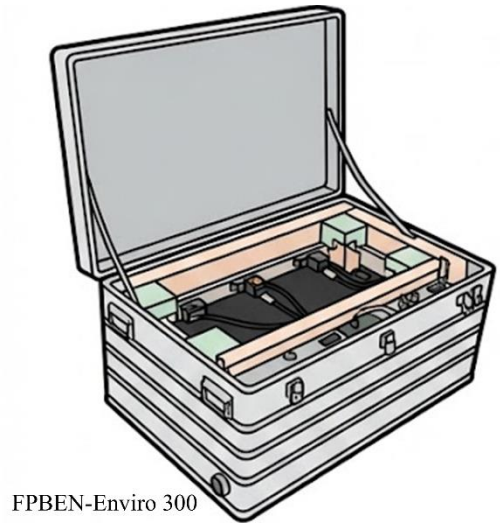
Supplementary Figure 12. In-situ thermal stability test of infrared light source chips. (A-D) Surface Morphologies of Suspended Membrane Infrared Light Source Chips at room temperature, 300 °C, 450 °C, and 600 °C; (E-H) Surface Morphologies of Suspended Membrane Infrared Light Source Chips at room temperature, 300 °C, 450 °C, and 600 °C.



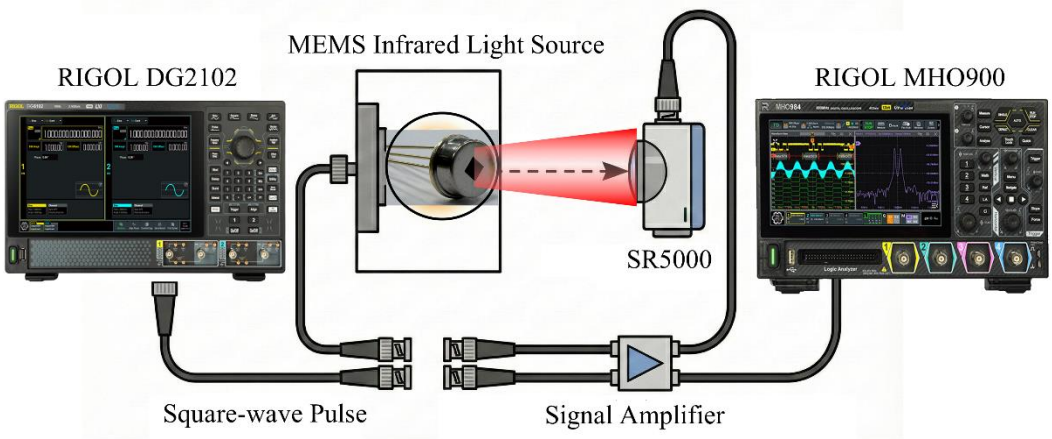
Supplementary Figure 13. Schematic diagram of thermal flux distribution for the semi-closed membrane infrared light source structure.



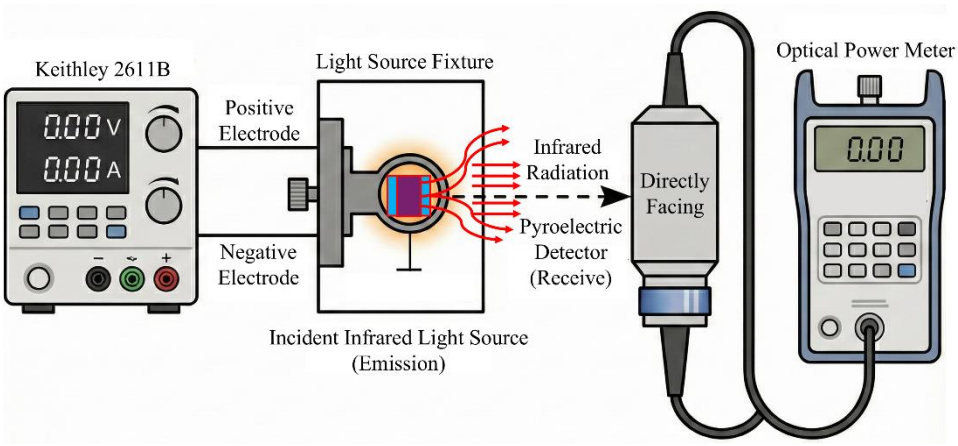
Supplementary Figure 14. Schematic diagram of the infrared emissivity test platform.



Supplementary Figure 15. Schematic of the FPBEN-Enviro 300 full-band solar spectral radiometer.



Supplementary Figure 16. Schematic diagram of the modulation performance test platform for the infrared light source.



Supplementary Figure 17. Schematic diagram of the test platform for electro-optical conversion efficiency of the infrared light source.